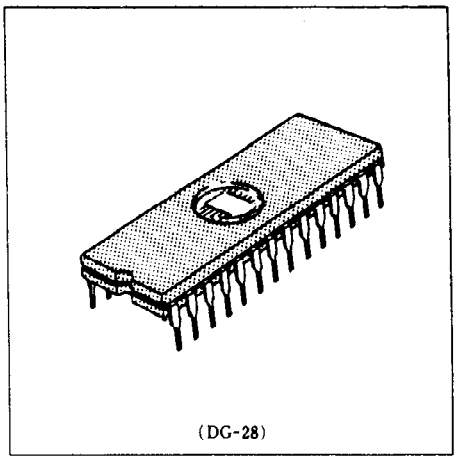
HN4827128G-25, HN4827128G-30, HN4827128G-45

Preliminary

16384-Word x 8-bit UV Erasable and Programmable Read Only Memory

The HN4827128 is a 16384 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

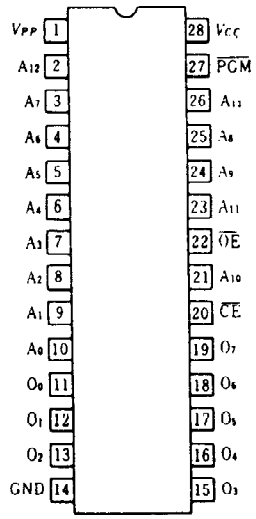


(DG-28)

■FEATURES

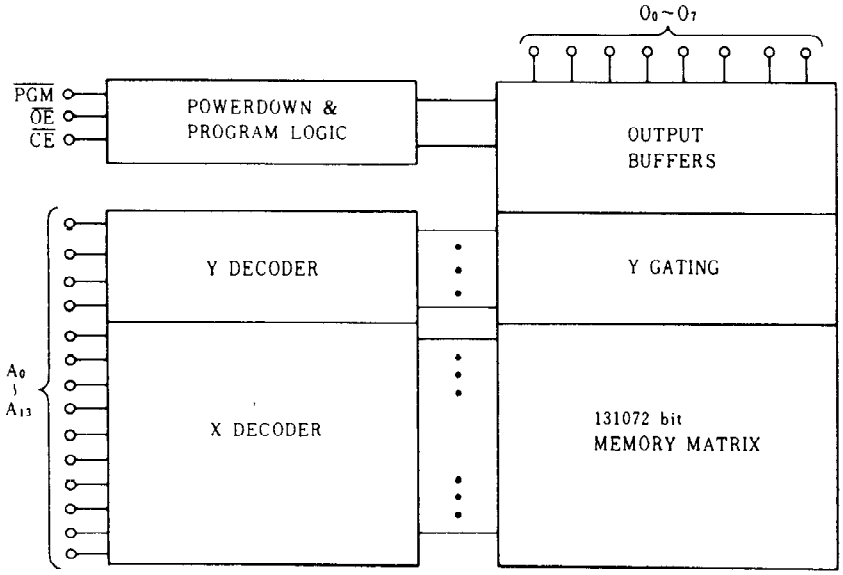
- Single Power Supply . . . . . +5V ± 5%
- Simple Programming . . . . . Program Voltage: +21V DC
  Program with One 50ms Pulse
- Static . . . . . No Clocks Required
  Inputs and Outputs TTL Compatible During Both Read and Program Mode.
- Access Time 250ns/300ns/450ns
- Absolute Max. Rating of Vpp Pin 26.5V
- Low Stand-by Current 35mA
- High Performance Programming Available
- Compatible with INTEL 27128

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■MODE SELECTION

MODE \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Stand by	V_{IH}	×	×	V_{CC}	V_{CC}	High Z
Program	V_{IL}	×	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	×	×	V_{PP}	V_{CC}	High Z

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■PROGRAMMING OPERATION

●DC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{IN}=5.25V	—	—	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH}=−400μA	2.4	—	—	V
V_{CC} Current (Active)	I_{CC2}		—	—	100	mA
Input Low Level	V_{IL}		−0.1	—	0.8	V
Input High Level	V_{IH}		2.0	—	V_{CC}+1	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$=$\overline{PGM}$=V_{IL}	—	—	30	mA

●AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VS}		2	—	—	μs
$\overline{PGM}$ Pulse Width During Programming	t_{PW}		45	50	55	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}		—	—	150	ns

Note : t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

●SWITCHING CHARACTERISTICS

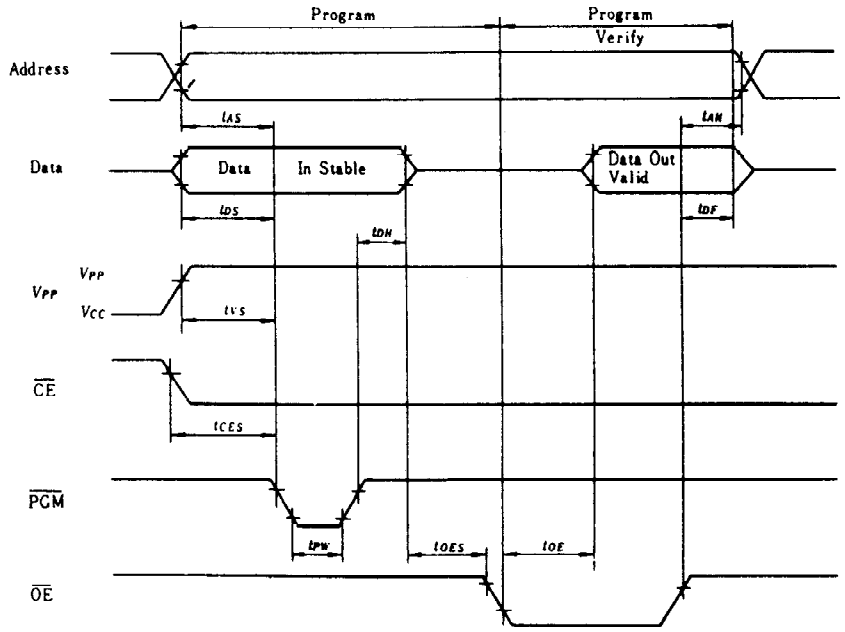
Test Condition

Input Pulse Level: 0.8V to 2.2V

Input Rise and Fall Time: ≤ 20 ns

Reference Level for Measuring Timing: Input; 1V and 2V

Output; 0.8V and 2V



●ERASE

Erasure of HN4827128 is performed by exposure to ultraviolet light of 2537Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15 W·sec/cm^2.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C
All Input and Output Voltages*	V_{IN}, V_{out}	−0.3 to +7	V
V_{PP} Voltage*	V_{PP}	−0.3 to +26.5	V
V_{CC} Voltage*	V_{CC}	−0.3 to +7	V

* with respect to GND

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{CC}=5.25V, V_{IN}=5.25V	—	—	10	μA
Output Leakage Current	I_{LO}	V_{CC}=5.25V, V_{out}=5.25V/0.4V	—	—	10	μA
V_{PP} Current	I_{PP1}	V_{PP}=V_{CC}+0.6V	—	—	5	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$=V_{IH}	—	—	35	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$=$\overline{OE}$=V_{IL}	—	60	100	mA
Input Low Voltage	V_{IL}		−0.1	—	0.8	V
Input High Voltage	V_{IH}		2.0	—	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	—	—	V

● AC CHARACTERISTICS (Ta=0 to 70°C, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

Parameter	Symbol	Test Condition	HN4827128G-25		HN4827128G-30		HN4827128G-45		Unit
			min	max	min	max	min	max	
Address to Output Delay	t_{ACC}	$\overline{CE}$=$\overline{OE}$=V_{IL}	—	250	—	300	—	450	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$=V_{IL}	—	250	—	300	—	450	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$=V_{IL}	—	100	—	120	—	150	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$=V_{IL}	0	85	0	105	0	130	ns
Address to Output Hold	t_{OH}	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	—	0	—	0	—	ns

* t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

Test Condition

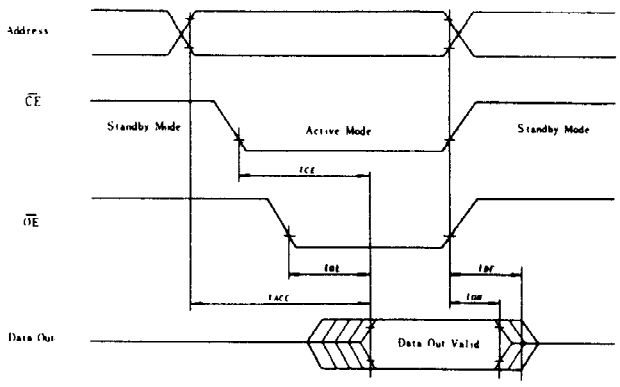
Input Pulse Levels: 0.8V to 2.2V

Input Rise and Fall Time: ≤ 20 ns

Output Load: 1 TTL Gate + 100 pF

Reference Level for Measuring Timing: Inputs; 1V and 2V

Outputs; 0.8V and 2.0V

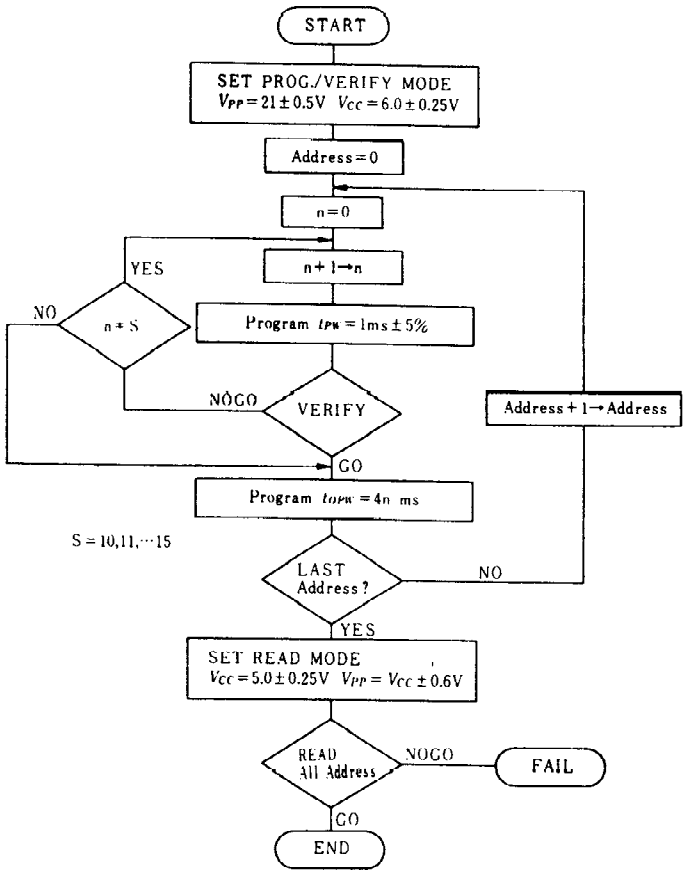


● CAPACITANCE (Ta=25°C, f= 1 MHz)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	—	4	6	pF
Output Capacitance	C_{out}	V_{out}=0V	—	8	12	pF

■HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flow chart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

● AC PROGRAMMING CHARACTERISTICS (Ta = 25°C ±5°C, V_{CC} = 6V±0.25V, V_{PP} = 21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay*	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VPS}		2	—	—	μs
V_{CC} Setup Time	t_{VCS}		2	—	—	μs
$\overline{PGM}$ Pulse Width during Initial Program	t_{PW}		0.95	1.0	1.05	ms
$\overline{PGM}$ Pulse Width during Over Program**	t_{OPW}		3.8	—	63	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}		—	—	150	ns

* t_{DF} defines the time at which the output achieves the open circuit conditions and is not referenced to output voltage levels.

** t_{OPW} is defined as mentioned in flow chart.

● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Time:	≤ 20 ns
Reference Level for Measuring Timing:	Input; 1V and 2V
	Output; 0.8V and 2V